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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/604,912
Filing Date: August 26, 2003
Appellant(s): PARK ET AL.

Pamela M. Riley, Esq.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 17, 2006 appealing from the Office action mailed July 5, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellants' statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellants' statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,429,084	Park et al.	8-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

A. **Claims 1, 2, 4-9, 11-17, 19-24 and 26-28 are stand rejected under 35 U.S.C. 102(b) as being anticipated by Park et al. (US/6,429,084).**

Re claim 1, park et al. disclose a method of forming an integrated circuit transistor having a reduced gate height, said method comprising: forming a laminated structure having a substrate (i.e., SOI substrate), a gate conductor (50) above the substrate (see Fig. 1), and at least one sacrificial layer (51 52 54) above the gate conductor (50); patterning the laminated structure into at least one gate stack (55) extending from the substrate (see Fig. 1) (Col. 1, lines 50-65); forming spacers (60 70) with a target spacer width adjacent to said gate stack (55) (see Fig. 2), wherein in order to achieve the target spacer width, a combined height of the gate conductor and the at least one sacrificial layer is predetermined ; doping regions of the substrate not protected by the spacers (60 70) with an impurity to form source and drain regions adjacent the gate stack (55); wherein the spacers with the target spacer width is predetermined to ensure the spacers

sufficiently separate the source drain regions form that gate stack so to avoid lateral encroachment of the impurity into a channel region below the gate stack regardless of a height of the gate conductor; and removing the spacers and the sacrificial layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 2, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein forming of the spacers adjacent the gate stack comprises forming of the spacers adjacent the gate conductor and at least on sacrificial oxide layer (54) above the gate conductor (50) (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 4, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein the forming of comprises the spacers so as to positions the source and drain regions further from the gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 5, The method in claim 1, wherein said sacrificial layer above said gate conductor is formed in a process comprising: forming a sacrificial oxide layer above said gate conductor, and forming additional sacrificial layers above said oxide layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 6, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 7, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a gate dielectric (40) below said gate conductor layer and a silicon layer (i.e., part of SOI) below said gate conductor (50),

wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and said gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 8, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a dielectric layer (40) below said gate conductor layer (50) a silicon layer below said gate dielectric layer (40), wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process, wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and aid gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 9, Park et al. disclose a method of forming an integrated circuit transistor having a reduced gate height, the method comprising: forming a laminated structure having a substrate (see Fig. 1), a gate conductor (50) above the substrate, and at least one sacrificial layer (54) above said gate conductor (see Fig. 1); patterning said laminated structure into at least one gat stack extending from said substrate; forming spacers with a target spacer width adjacent to

the gate stack wherein in order to achieve the target spacer width, a combined height of the gate conductor and the at least one sacrificial layer is predetermined; epitaxially growing raised source and drain regions on said substrate adjacent said gate stack (see Fig. 5); after said epitaxially growing of said raised source drain regions, implanting an impurity into said raised source and drain regions and into said substrate below the raised source drain regions (see Figs. 9 and 10); wherein implanting said impurity after said epitaxially growing and raised source drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said target spacer width is predetermined to ensure the spacers sufficiently separate the raised source drain regions form the gate stack so as to avoid lateral encroachment of the impurity unto a channel region below the gate stack regardless of a height of the gate conductor; and removing said spacers and said sacrificial layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 11, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein the forming the spacers comprises forming of the spacers with target spacer width so as to positions said raised source and drain regions further from said gate conductor when compared to raised source and drain regions formed with spacers formed only to said height of said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 12, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial layer above said gate conductor is formed in a process comprising: forming a sacrificial oxide layer above said gate conductor, and forming additional sacrificial layers above said oxide layer, wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 13, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a gate dielectric (40) below said gate conductor layer and a silicon layer (i.e., part of SOI) below said gate conductor (50), wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and said gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 14, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a dielectric layer (40) below said gate conductor layer (50) a silicon layer below said gate dielectric layer (40), wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process, wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and aid gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 15, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein by implanting said impurity after said epitaxially growing

process, said impurity avoid being diffused as result of said thermal budget of said epitaxially growing process (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 16, Park et al. disclose a method of forming an integrated circuit transistor having a reduced gate height, said method comprising: forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor; patterning said laminated structure into at least one gate stack extending from said substrate; forming spacers with a target spacer width adjacent said gate stack, wherein in order to achieve the target spacer width, a combined height of the gate conductor and the at least one sacrificial layer is predetermined; epitaxially growing raised source and drain regions on said substrate adjacent said spacers, wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities; after said epitaxially growing of said raised source drain regions, implanting impurities into said raised source and drain regions and into said substrate below the raised source drain regions (see Figs. 9 and 10); wherein implanting said impurities after said epitaxially growing and raised source drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said target spacer width is predetermined to ensure the spacers sufficiently separate the raised source drain regions form the gate stack so as to avoid lateral encroachment of the impurity unto a channel region below the gate stack regardless of a height of the gate conductor; and removing said spacers and said sacrificial layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 17, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein forming of the spacers adjacent the gate stack comprises

forming of the spacers adjacent the gate conductor and at least on sacrificial oxide layer (54) above the gate conductor (50) (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 19, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein the forming the spacers comprise forming the spacers with target spacer so as to positions said source and drain regions further from said gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 20, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial layer above said gate conductor is formed in a process comprising: forming a sacrificial oxide layer above said gate conductor, and forming additional sacrificial layers above said oxide layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 21, as applied to claim 20 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 22, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a gate dielectric (40) below said gate conductor layer and a silicon layer (i.e., part of SOI) below said gate conductor (50), wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and whereas, without said sacrificial layer, said doping process would

implant an impurity through said gate conductor and said gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 23, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a gate dielectric (40) below said gate conductor layer and a silicon layer below said gate dielectric layer , wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity that used in said first doping process after said first doping process, wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 24, Park et al. disclose a method of producing an integrated circuit transistor comprising: forming a laminated stack deposition, wherein said laminated stack deposition is formed in a process comprising: forming a silicon layer over a substrate layer (30) (i.e., part of SOI); forming a gate oxide (40) on said silicon layer (30); forming a gate conductor (50) on said gate oxide (40); and forming of least one sacrificial material above said gate conductor, patterning said gate oxide (see Figs. 5 and 6), gate conductor, and said sacrificial material into at least one gate stack (see Figs. 1-6); forming temporary spacers (70 60) with a target width adjacent said gate stack (55), wherein in order to achieve the target spacer width, a combined height of the gate conductor and the at least one sacrificial layer is predetermined; epitaxially

growing raised source and drain regions (36) (see Fig. 6) above said substrate layer adjacent said temporary spacers, such that said temporary spacers separate said raised source and drain regions from said gate stack, wherein the epitaxially growing process of the raised source and drain regions performed in the absence of doping of impurities; simultaneously implanting impurities into said raised source and drain regions and into said substrate below the raised source drain regions (see Figs. 9 and 10); wherein implanting said impurities after said epitaxially growing and raised source drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said target spacer width is predetermined to ensure the spacers sufficiently separate the raised source drain regions form the gate stack so as to avoid lateral encroachment of the impurity into a channel region below the gate stack regardless of a height of the gate conductor; growing an additional dielectric layer (44) (see Fig. 8) on said raised source and drain regions (36); removing said temporary spacers (see Fig. 9) without removing said sacrificial material (51); performing a halo implant (see Fig. 10) in said raised source and drain regions and in exposed regions of said silicon layer; forming a permanent spacer (80) (see Fig. 11) adjacent said gate stack, wherein said permanent spacer is thinner than said temporary spacer; performing a source and drain extensions implant in said raised source and drain regions and exposed regions of said silicon; forming a final spacer filling said exposed regions of said silicon between said permanent spacer and said raised source and drain regions; implanting additional impurity into said raised source and drain regions and exposed regions of said silicon; annealing to activate all impurity; etching back said additional dielectric layer on said raised source and drain regions; and saliciding both said gate conductor and said raised source and drain regions (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 26, as applied to claim 24 above, Park et al. disclose all the claimed limitations including the limitation wherein said removing of said sacrificial layer reduces the height of said gate conductor relative to the gate height associated with the spacing of the source and drain regions created by said spacers (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 27, as applied to claim 24 above, Park et al. disclose all the claimed limitations including the limitation wherein said forming of said sacrificial material above said gate conductor further comprises forming a sacrificial oxide layer above said gate conductor, forming a sacrificial nitride layer above said oxide layer and forming a sacrificial hard insulator material above said nitride layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 28, as applied to claim 24 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

(10) Response to Argument

Appellants' arguments in the appeal brief filed on November 17, 2006 have been fully considered but they are not persuasive.

A.

Pertaining rejection of claims 1, 9, 16 and 24, Appellants argue that "Park does not teach or suggest forming spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width a combined height of said gate conductor and said at least one sacrificial layer is predetermined and wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said source and drain regions from said gate stack

so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor..." (See Appellants' arguments in Page 22).

In response Appellants' contention, it is respectfully submitted that Park et al. '084 disclose all the claimed limitations including "*forming spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width a combined height of said gate conductor and said at least one sacrificial layer is predetermined and wherein said target spacer width is predetermined to ensure that said spacers sufficiently separate said source and drain regions from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor*" as set froth above.

The following drawings of Park et al. '084 respectfully submitted for demonstrative purpose:

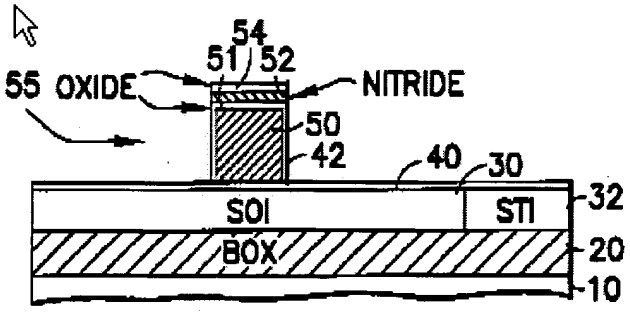

FIG. 1

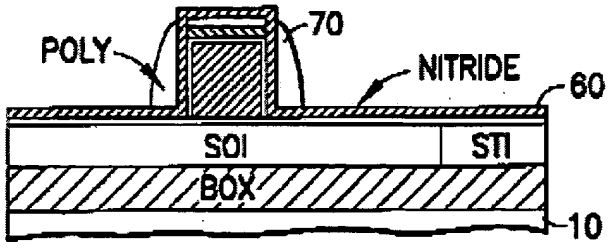

FIG.2

As shown in Figs. 1 and 2 above, Park et al. discloses forming of spacers **42 70** with a target spacer **60** adjacent the gate stack **50 51 52 54.**

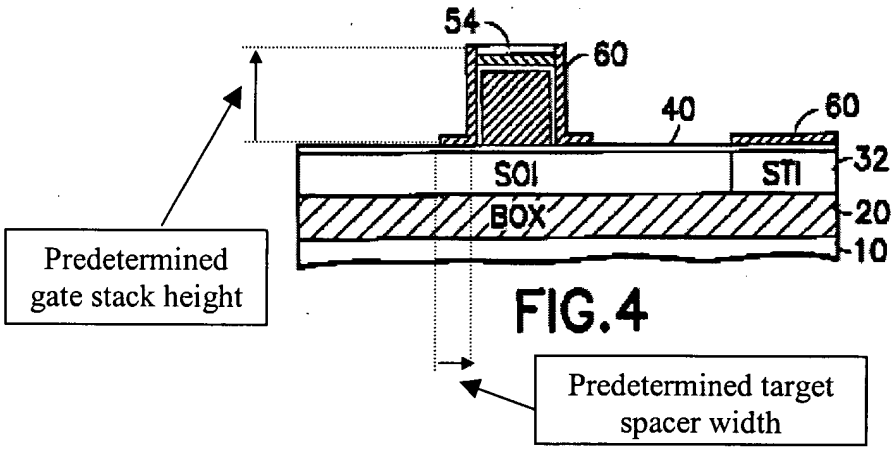

FIG.4

In the subsequent process, as shown Fig. 4 above, the target spacer **60** has a predetermined width and ensures that the spacers **60 42** sufficiently separates the source **40** and drain **34**, as shown in Fig. 5 below.

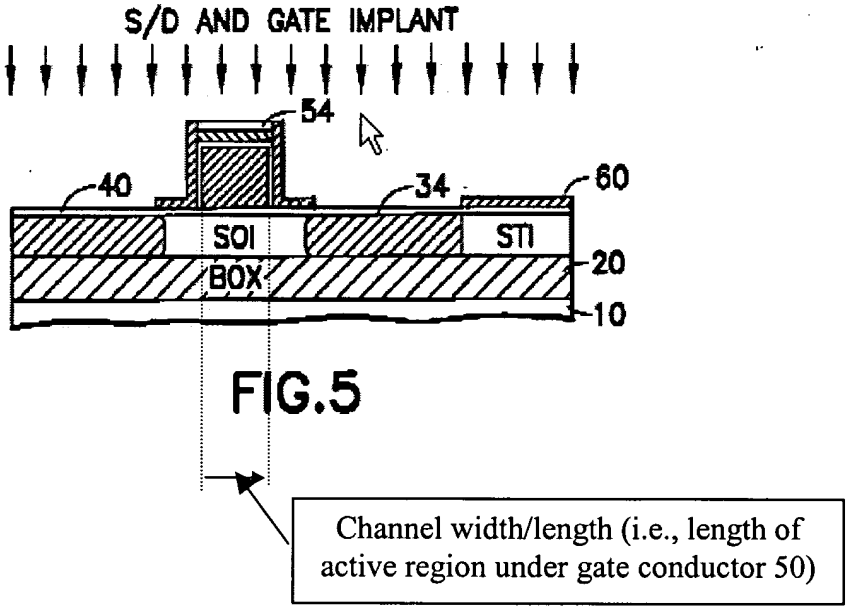

FIG.5

Further, as clearly shown in Fig. 5, no lateral encroachment occurred into the channel region (i.e., the region under the gate and diffusion of the dopants from the source drain region into the channel region is avoided due to the predetermined length of the target spacer **60** as shown in Fig. 5).

In addition, the rejected claims, i.e., claims 1, 9, 16 and 24, are broad and are clearly anticipated by Park et al. '084 because there is no material or process distinction can be made between the rejected claims and Park et al. '084 disclosure. The use of spacers on the sidewalls of the gate electrode is well-known in the art and has been routinely used during formation source drain regions in order to avoid lateral diffusion of the dopant into the channel region which causes short circuiting of the device. As shown in Fig. 5 above, the structure clearly inherently avoids lateral encroachment of the dopant impurity into a channel region below the gate stack regardless of a height of the gate conductor.

The Examiner gives claims their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28

(Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Therefore, the rejection of claims 1, 9, 16 and 24 under 35 U.S.C. §102 (b) is deemed proper.

B.

Pertaining claims 9,16 and 24, Appellants further argue, "Park does not teach or suggest, after said epitaxially growing of said raised source and drain regions, implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions..." (See the brief in last line of Page 22 through first Paragraph of Page 23).

In response to Appellants' argument, it is respectfully submitted that Park et al. '084 disclose all the claimed limitations of claims 9, 16 and 24 including "*after said epitaxially growing of said raised source and drain regions, implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions, wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process*."

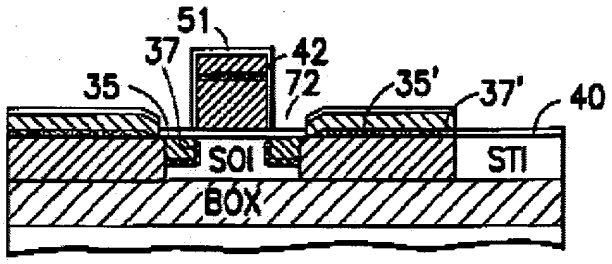

FIG. 10

As shown in Fig. 10, the halo implant region **35 37** formed into the substrate below the top portion of the source **34** and drain **40** regions or below raised/source drain regions during the formation of the halo implant region the epi layer (epitaxial layer) **36** (i.e., the epi layer 36 also known as raised source and drain) is simultaneously implanted in order to provide dopant (impurity) in the epitaxial layer **36** (Note Col. 2, lines 60-67). As well known in the art, the objective of the halo implantation is providing a deep penetration of the dopant into the silicon surface without requiring additional heating or annealing process. This process is commonly known as reduction or limitations of thermal budget.

Furthermore, there is no implicit or explicit suggestion or evidence can be found in the Park et al. '084 disclosure that annealing of the device after the halo implantation. Park et al. '084 further suggest that "those skilled in the art will be able to appreciate that various modifications of the disclosed process may be made. For example, nitride 60 may be made thinner and spacers 70 used to block the area where the halo and extension implants will be. Further, the conventional order for the implants first extension and halo, then S/D may be used, **at the cost of greater thermal spread of the small implants**. The annealing of the S/D could be done at any time after their implantation." (Note Park et al. Col. 3, lines 20-29). In other words, Park et al. halo implant process of the epi layer **36** (i.e., raised source/drain) is intended to avoid

subjecting the impurity to the thermal budget of the epitaxially growing process. Hence, the halo implantation of the epitaxial layer **36** and into the substrate to form halo regions provides *implanting an impurity* **35' 37'** *into the raised source and drain regions and into the substrate below the raised source and drain regions, wherein implanting the impurity after the epitaxially growing of the raised source and drain regions avoids subjecting the impurity to the thermal budget of the epitaxially growing process* as clearly disclosed by Park et al. '084.

C.

With respect to Appellants' argument that "*Park also does not teach or suggest said process of epitaxially growing said source drain region is performed in the absence of doping impurities*," it is respectfully submitted that, unless it is specified, the epitaxial layer is commonly grown without impurities and there is no implicit or explicit evidence that the epitaxial layer **36** in Park et al. disclosure has been grown with the presence of impurities (i.e., in presence of dopants). Normally, *in situ* doping is performed to provide the dopant in the epitaxial layer during deposition process of epitaxial growth of silicon or silicon germanium in order to avoid further doping step. Contrary to Appellants' argument, the purpose of ion implantation the epi layer **36** by implanting an impurity **35' 37'** into the raised source and drain regions is an implicit evidence that the epi layer **36** indeed grown in the absence of doping and the formation of impurity region **35' 37'** in the epi layer **36** is done to provide the necessary impurity in the epi layer **36** during formation of raised source/drain regions.

Therefore, the rejection of claims 9, 16 and 24under 35 U.S.C. §102 (b) is deemed proper in this aspect.

Further, Appellants' position and contention, as set forth in the Brief, in the second paragraph of Page 23 through out Page 34, is noted. However, the arguments and Appellants'

position basically repetitive and it dose not present different argument that requires response by the Examiner and it is respectfully submitted all the issues have been addressed here in above.

D.

Finally, with respect to dependent claims, i.e., claims 2, 4-8, 11-15, 17, 19-23, and 26-28, Appellants did not present separate and/or independent arguments. Therefore, it is respectfully submitted that claims 2, 4-8, 11-15, 17, 19-23, and 26-28 should stand or fall with the base independent claims.

For the above reasons, it is believed that the rejections should be sustained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Respectfully submitted,

Brook Kebede

BROOK KEBEDE
PRIMARY EXAMINER

Appeal conference has been held on January 18, 2007. The Conferees listed herein below.

1. Ricky L. Mack, Chair Person and SPE Art Unit 2873. RM
2. Matthew S. Smith, SPE Art Unit 2823. Matthew S. Smith
3. Brook Kebede, Examiner Art Unit 2823. BK

BK
January 26, 2007